CLAIMS

What is claimed is:

1   1.   A method comprising:

2   evaluating one or more source characters to determine whether each

3   character will invert or maintain a current running disparity; and

4   determining a running disparity for each character before encoding the

5   character based on the current running disparity and whether the character will

6   invert or maintain the current running disparity.

1   2.   The method of claim 1, wherein evaluating one or more source characters

2   comprises evaluating each source character to determine a flip/hold bit based on

3   whether the character will invert or maintain a current running disparity.

1   3.   The method of claim 2, wherein determining a running disparity for each

2   character comprises comparing the flip/hold bit of each character with the current

3   running disparity.

1   4.   The method of claim 3, wherein determining a running disparity for each

2   character comprises using an exclusive or (XOR) function to compare the flip/hold bit

3   with the current running disparity.

1   5.   The method of claim 1, wherein evaluating one or more source characters

2   comprises using a lookup table to determine whether each source character will invert

3   or maintain the current running disparity.

1 6.   The method of claim 1, wherein evaluating one or more source characters

2 comprises using one or more logic gates to determine whether each source character

3 will invert or maintain the current running disparity.

1 7.   The method of claim 1, further comprising passing the current running disparity

2 along with the associated source character to an encoder to encode the source

3 character into a transmission character.

1 8.   A circuit comprising:

2   a decoder to determine a flip/hold bit based on whether a source character

3 will invert or maintain a current running disparity; and

4   a comparator coupled to the decoder to compare the flip/hold bit with the

5 current running disparity to determine a running disparity for the source character

6 before the source character is encoded.

1 9.   The circuit of claim 8, wherein the comparator comprises one or more

2 exclusive or (XOR) gates.

1 10.   The circuit of claim 8, wherein the comparator comprises a pre-calculator to

2 pre-calculate at least a portion of the running disparity.

1 11.   The circuit of claim 10, wherein the pre-calculator comprises one or more

2 exclusive or (XOR) gates.

1 12.   The circuit of claim 8, further comprising an encoder coupled to the comparator

2 to receive the current running disparity and the associated source character and to

3 encode the source character to a transmission character.

1   13.   The circuit of claim 12, wherein the encoder is an 8B/10B encoder that does

2   not contain disparity calculation circuitry.

1   14.   An apparatus comprising:

2   means for evaluating one or more source characters to determine a flip/hold

3   bit based on whether each source character will invert or maintain a current running

4   disparity; and

5   means for comparing the flip/hold bit of each source character with the

6   current running disparity to determine a running disparity for each source character

7   before the source character is encoded.

1   15.   The apparatus of claim 14, wherein the means for comparing the flip/hold bit

2   with the current running disparity comprises one or more exclusive or (XOR) gates.

1   16.   The apparatus of claim 14, wherein the means for comparing the flip/hold bit

2   with the current running disparity comprises means for pre-calculating at least a

3   portion of the running disparity.

1   17.   The apparatus of claim 14, wherein the means for evaluating the one or more

2   source characters comprises one or more lookup tables.

1   18.   The apparatus of claim 14, wherein the means for evaluating the one or more

2   source characters comprises one or more logic gates to determine whether each

3   source character will invert or maintain the current running disparity.

1   19.   The apparatus of claim 14, further comprising an encoder coupled to the

2   comparing means to receive the running disparity and the associated source

3   character and to encode the source character to a transmission character.

1   20.   The apparatus of claim 19, wherein the encoder is an 8B/10B encoder that

2   does not contain disparity calculation circuitry.